Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A synchroniser for use in a receiver which receives signals, said synchroniser comprising:

means for providing a digital control signal, said control signal defining a plurality of different levels;

means for controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values; and

means for estimating the difference between the levels of successive ones of said control signals.

2. (Original) A synchroniser as claimed in claim 1, wherein said digital control signal is converted into an analogue control signal.

3. (Previously presented) A synchroniser as claimed in claim 1, wherein said providing means, said controlling means and said estimating means are in the digital domain.

4. (Original) A synchroniser as claimed in claim 3, wherein said providing means, said controlling means and said estimating means are provided in a digital signal processor.

5. (Previously presented) A synchroniser as claimed in claim 1, wherein said providing means comprises a digital corrector.

6. (Previously presented) A synchroniser as claimed in claim 1, wherein a rough correction is provided by said control signal.

7. (Currently Amended) A synchroniser as claimed in claim 6 ~~7~~, wherein a rough correction is provided in an analogue domain.

8. (Previously presented) A synchroniser as claimed in claim 6, wherein a finer correction is provided.

9. (Original) A synchroniser as claimed in claim 8, wherein said finer correction is provided in a digital domain.

10. (Previously presented) A synchroniser as claimed in claim 1, wherein said means for estimating comprises an estimator arranged to determine that the difference between two successive levels has increased if a difference between the upper of said levels and an estimated level for an actual signal provides a signal at a higher level than a signal provided by a difference between a lower of said levels and an estimated level for the actual signal.

11. (Previously presented) A synchroniser as claimed in claim 2, wherein said means for estimating comprises an estimator arranged to determine that the difference between

two successive levels has increased if a difference between the upper of said levels and an estimated level for an actual signal provides a signal at a higher level than a signal provided by a difference between a lower of said levels and an estimated level for the actual signal.

12. (Previously presented) A synchroniser as claimed in claim 1, wherein said means for estimating comprises an estimator arranged to determine that an actual signal has changed if a difference between the upper of said levels and an actual signal provides a signal at substantially the same level as a signal provided by a difference between a lower of said levels and the actual signal, said same level being different to a previous level for said actual signal.

13. (Previously presented) A synchroniser as claimed in claim 1, wherein said synchroniser is arranged to at least one of acquire and track frequency error.

14. (Previously presented) A synchroniser as claimed in claim 1, wherein said synchroniser is arranged to at least one of acquire and track timing error.

15. (Previously presented) A receiver comprising a synchroniser as claimed in claim 1.

16. (Original) A receiver as claimed in claim 15, wherein said control signal is used to control a mixing frequency.

17. (Previously presented) A synchroniser as claimed in claim 2, wherein said providing means, said controlling means and said estimating means are in the digital domain.

18. (Previously presented) A synchroniser as claimed in claim 7, wherein a finer correction is provided.

19. (New) A receiver as claimed in claim 15, further comprising:

an antenna for receiving signals;

a first bandpass filter for filtering out unwanted signals;

a mixer for downconverting received signals to a baseband frequency;

a second bandpass filter for removing unwanted signals falling outside the bandwith of said second bandpass filter;

an analogue to digital converter for converting signals received from said second bandpass filter from analogue to digital form; and

a digital to analogue converter for converting the signals received from said digital signal processor from digital to analogue form.

20. (New) A receiver as claimed in claim 19, wherein said synchroniser includes a digital signal processor comprising:

a detector for measuring frequency errors and sending a digital word;

a filter for filtering said digital word output by said detector;

a step size estimator for estimating an actual step size of a frequency change provided by said digital to analogue converter and providing said actual step size to analogue correction; and

a digital automatic frequency control unit for controlling division of correction between analogue and digital parts, performing an accurate correction so that a zero or close to zero error is achieved and compensating for the effect of an analogue control for which a step size is estimated while a control word is changed;

21. (New) A method for providing synchronization in a receiver, comprising the steps of:

providing a digital control signal, said control signal defining a plurality of different levels;

controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values; and

estimating the difference between the levels of successive ones of said control signals.